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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,370	10/09/2003	Seiji Yamahira	43890-633	6387

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Washington, DC 20005-3096

EXAMINER

NGUYEN, MINH T

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

Office Action Summary

Application No.

10/681,370

Applicant(s)

YAMAHIRA ET AL.

Examiner

Minh Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) 6 and 9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 7 is/are rejected.
- 7) ☒ Claim(s) 2-5 and 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/9/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Applicants' election of group I without traverse filed on 1/21/05 is acknowledged. The following is a detailed Office action of the selected group, i.e., claims 1-5 and 7-8. The non-elected species, i.e., claims 6 and 9 can be requested to rejoin later if the generic claims are found allowable.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it uses words which can be implied, i.e., "is provided", "of the present invention", "comprises". Correction is required. See MPEP § 608.01(b).

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested:
Level Shift Circuit having Control Circuits for High Speed and Power Saving.

4. The disclosure is objected to because of the following informalities: the Summary of Invention should not be a copy version of the claims. Appropriate correction is required.

Claim Objections

5. Claims 1 and 7 are objected to because of the following informalities:

In claim 1, lines 13 and 16, "turen ON" should be changed to -- turn ON --.

In claim 7, the same problems exist as discussed in claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,373,315, issued to Tsuji et al.

As per claim 1, Tsuji discloses a level shift circuit (Fig. 6), comprising:

a first conduction type first transistor (NMOS 10) wherein a first power source voltage (GND) is supplied to a source, a first input signal (the input signal at the output of inverter 1) is applied to a gate, and a first terminal (the terminal at node N6) is connected to a drain;

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a first conduction type second transistor (NMOS 11) wherein a second input signal (the input signal at the output of inverter 2) in reverse relation to the first input signal (inverted by the inverter 2) is applied to a gate, and a drain is connected to a second terminal (the terminal at node N7);

a second conduction type third transistor (PMOS 16) wherein a second power source voltage (VPP) is supplied to a source, and the first terminal is connected to a drain (at node N6);

a second conduction type fourth transistor (PMOS 7) wherein the second terminal is connected to a drain (at node N7);

a first gate voltage control circuit (the combination of FETs 4, 5, 8 and 9) connected to the second terminal (the gate of FET 8 is connected to node N7), input the second input signal (at the gate of FET 9), and making said third transistor turn ON when said first transistor is OFF (Fig. 7, see graphs $\phi(1)$ and N7, i.e., a LOW of $\phi(1)$ turns OFF NMOS 10 and a LOW of N7 turns ON PMOS 16); and

a second gate voltage control circuit (the combination of FETs 14, 15, 18 and 19) connected to the first terminal (the gate of FET 18 is connected to node N6), input the first input signal (at the gate of FET 19), and making said fourth transistor turn ON when said second transistor is OFF (see Fig. 7).

As per claim 7, Tsuji discloses a level shift circuit (Fig. 6), comprising:

a first conduction type second transistor (NMOS 11) wherein a first power source voltage (GND) is supplied to a source, a second input signal ($\phi(2)$) in reverse relation to a first input signal ($\phi(1)$) is applied to a gate, and a drain is connected to a second terminal (N7);

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a second conduction type fourth transistor (PMOS 7) wherein a second power source voltage (VPP) is supplied to a source, and the second terminal is connected to a drain;

a second conduction type thirteenth transistor (PMOS 16) wherein the second power source voltage is supplied to a source;

a third gate voltage control circuit (the combination of FETs 4, 5, 8 and 9) connected to the second terminal (at node N7), input the second input signal (at the gate of FET 9), and making said thirteenth transistor turn ON when the second input signal is at a high level (see Fig. 7, when the second input signal is HIGH, the voltage at the gate of the thirteenth transistor is LOW); and

a fourth gate voltage control circuit (the combination of FETs 14, 15, 18 and 19) connected to a drain of said thirteenth transistor (at node N6), input the first input signal, and making said fourth transistor turn ON when the first input signal is at a high level (see Fig. 7).

Allowable Subject Matter

7. Claims 2-5 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-3 are allowable because the prior art of record fails to disclose or suggest the inclusion of a first and second control circuits wherein each of the control circuits includes transistors configured as recited in claim 2.

Claim 4 is allowable for the same reason noted in claim 2.

Claim 5 is allowable because the prior art of record fails to disclose or suggest the inclusion of first and second switching circuits configured as recited in the claim.

Claim 8 is allowable because the prior art of record fails to disclose or suggest the inclusion of a switching circuit configured as recited in the claim.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



2/3/05

Minh Nguyen
Primary Examiner
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